# MOSFET

Metal Oxide Semiconductor Field Effect Transistor

# CoolMOS™ CFD2 650V

650V CoolMOS™ CFD2 Power Transistor
IPW65R080CFD

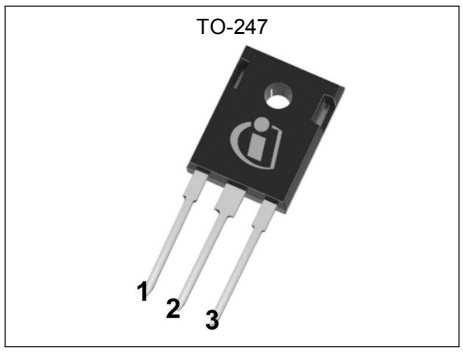
## Data Sheet

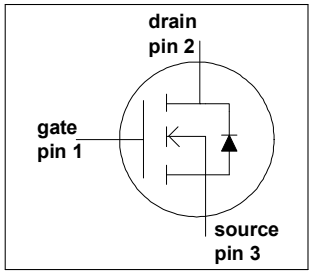
Rev. 2.4
Final

## Industrial & Multimarket

# 1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFD2 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter and cooler.




## Features

- Ultra-fast body diode
- Very high commutation ruggedness
- Extremely low losses due to very low FOM Rdson*Qg and Eoss
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

## Applications

650V CoolMOS™ CFD2 is especially suitable for resonant switching PWM stages for e.g. PC Silverbox, LCD TV, Lighting, Server,Telecom and Solar.

### Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ @ $T_{j\ max}$ | 700 | V |
| RDS(on),max | 0.08 | Ω |
| Qg,typ | 167 | nC |
| ID,pulse | 137 | A |
| Eoss @ 400V | 12.5 | µJ |
| Body diode di/dt | 900 | A/µs |
| Qrr | 1 | µC |
| trr | 180 | ns |
| Irrm | 10 | A |

| Type / Ordering Code | Package | Marking | Related Links |
|---|---|---|---|
| IPW65R080CFD | PG-TO 247 | 65F6080 | see Appendix A |

## Table of Contents

## 2 Maximum ratings

at $T_j$ = 25°C, unless otherwise specified

### Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current[1] | $I_D$ | | | 43.3 | A | $T_C$ = 25°C |
| | | | | 27.4 | | $T_C$ = 100°C |
| Pulsed drain current[2] | $I_{D,pulse}$ | | | 137 | A | $T_C$ = 25°C |
| Avalanche energy, single pulse | $E_{AS}$ | | | 1160 | mJ | $I_D$ = 8.7A, $V_{DD}$ = 50V |
| Avalanche energy, repetitive | $E_{AR}$ | | | 1.76 | mJ | $I_D$ = 8.7A, $V_{DD}$ = 50V |
| Avalanche current, repetitive | $I_{AR}$ | | | 8.7 | A | |
| MOSFET dv/dt ruggedness | dv/dt | | | 50 | V/ns | $V_{DS}$ = 0 ... 400V |
| Gate source voltage | $V_{GS}$ | -20 | | 20 | V | static |
| | | -30 | | 30 | | AC (f > 1 Hz) |
| Power dissipation (non FullPAK)<br>TO-247 | $P_{tot}$ | | | 391.0 | W | $T_C$ = 25°C |
| Operating and storage temperature | $T_j$, $T_{stg}$ | -55 | | 150 | °C | |
| Mounting torque (non FullPAK)<br>TO-247 | | | | 60 | Ncm | M3 and M3.5 screws |
| Continuous diode forward current | $I_S$ | | | 43.3 | A | $T_C$ = 25°C |
| Diode pulse current | $I_{S,pulse}$ | | | 140 | A | $T_C$ = 25°C |
| Reverse diode dv/dt[3] | dv/dt | | | 50 | V/ns | $V_{DS}$ = 0 ... 400V, $I_{SD} \le I_D$, $T_j$ = 25°C |
| Maximum diode commutation speed | $di_f/dt$ | | | 900 | A/µs | |

[1] Limited by $T_{j\,max}$.
[2] Pulse width $t_p$ limited by $T_{j\,max}$
[3] $V_{peak}<V_{(BR)DSS}$, $T_j<T_{j\,max}$, identical low and high side switch with same Rg

## 3 Thermal characteristics

**Table 3 Thermal characteristics TO-247**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | $R_{thJC}$ | | | 0.32 | °C/W | |
| Thermal resistance, junction - ambient | $R_{thJA}$ | | | 62 | °C/W | leaded |
| Soldering temperature, wavesoldering only allowed at leads | $T_{sold}$ | | | 260 | °C | 1.6 mm (0.063 in.) from case for 10s |

# 4 Electrical characteristics

at $T_j$ = 25°C, unless otherwise specified

## Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 650 | | | V | $V_{GS}$ = 0V, $I_D$ = 1mA |
| Gate threshold voltage | $V_{GS(th)}$ | 3.5 | 4 | 4.5 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 1.8mA |
| Zero gate voltage drain current | $I_{DSS}$ | | | 2 | µA | $V_{DS}$ = 650V, $V_{GS}$ = 0V, $T_j$ = 25°C |
| | | | 500 | | | $V_{DS}$ = 650V, $V_{GS}$ = 0V, $T_j$ = 150°C |
| Gate-source leakage current | $I_{GSS}$ | | | 100 | nA | $V_{GS}$ = 20V, $V_{DS}$ = 0V |
| Drain-source on-state resistance | $R_{DS(on)}$ | | 0.072 | 0.08 | Ω | $V_{GS}$ = 10V, $I_D$ = 17.6A, $T_j$ = 25°C |
| | | | 0.187 | | | $V_{GS}$ = 10V, $I_D$ = 17.6A, $T_j$ = 150°C |
| Gate resistance | $R_G$ | | 0.7 | | Ω | $f$ = 1MHz, open drain |

## Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | | 5030 | | pF | $V_{GS}$ = 0V, $V_{DS}$ = 100V, $f$ = 1MHz |
| Output capacitance | $C_{oss}$ | | 215 | | pF | |
| Effective output capacitance, energy related[1)] | $C_{o(er)}$ | | 158 | | pF | $V_{GS}$ = 0V, $V_{DS}$ = 0 ... 400V |
| Effective output capacitance, time related[2)] | $C_{o(tr)}$ | | 794 | | pF | $I_D$ = constant, $V_{GS}$ = 0V, $V_{DS}$ = 0 ... 400V |
| Turn-on delay time | $t_{d(on)}$ | | 20 | | ns | $V_{DD}$ = 400V, $V_{GS}$ = 13V, $I_D$ = 26.3A, $R_G$ = 1.8Ω |
| Rise time | $t_r$ | | 18 | | ns | |
| Turn-off delay time | $t_{d(off)}$ | | 85 | | ns | |
| Fall time | $t_f$ | | 6 | | ns | |

## Table 6 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | | 32 | | nC | $V_{DD}$ = 480V, $I_D$ = 26.3A, $V_{GS}$ = 0 to 10V |
| Gate to drain charge | $Q_{gd}$ | | 87 | | nC | |
| Gate charge total | $Q_g$ | | 167 | | nC | |
| Gate plateau voltage | $V_{plateau}$ | | 6.4 | | V | |

[1)] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 400V

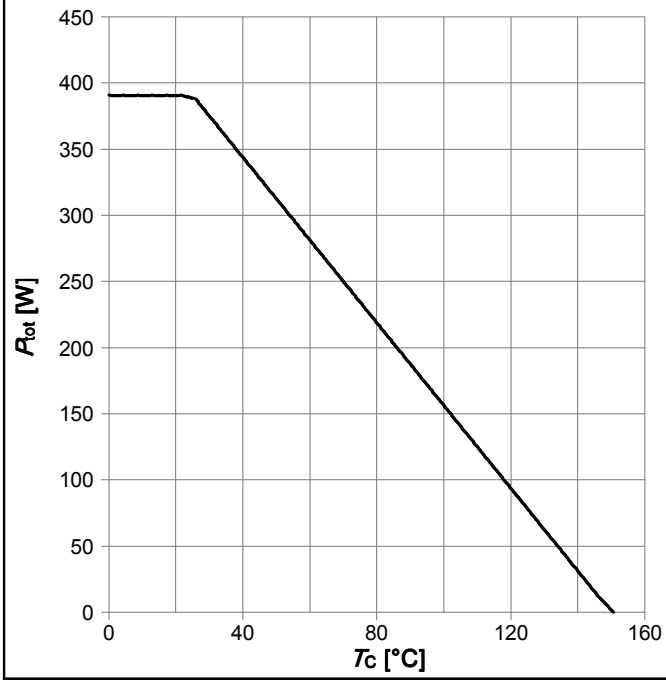
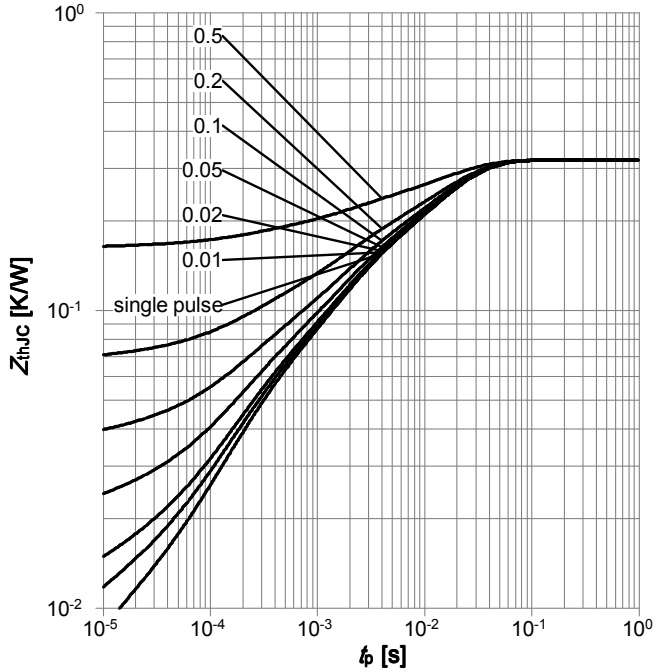
[2)] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 400V

**Table 7 Reverse diode characteristics**

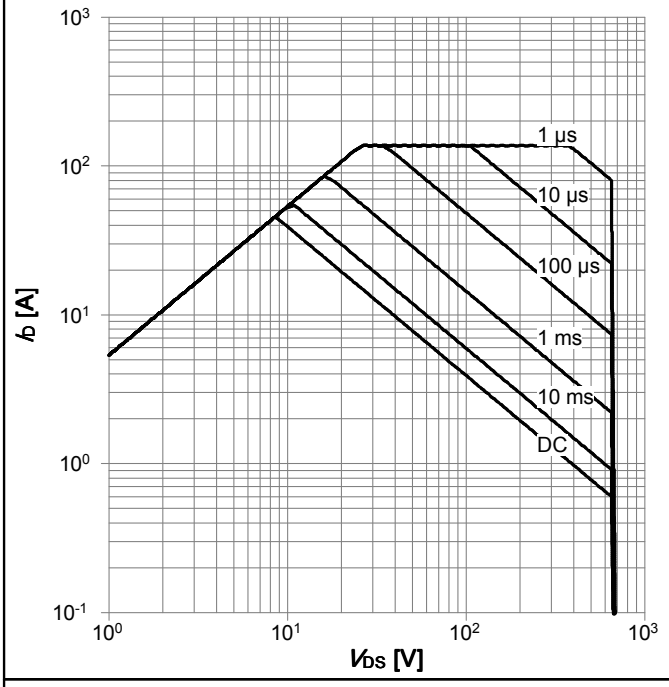
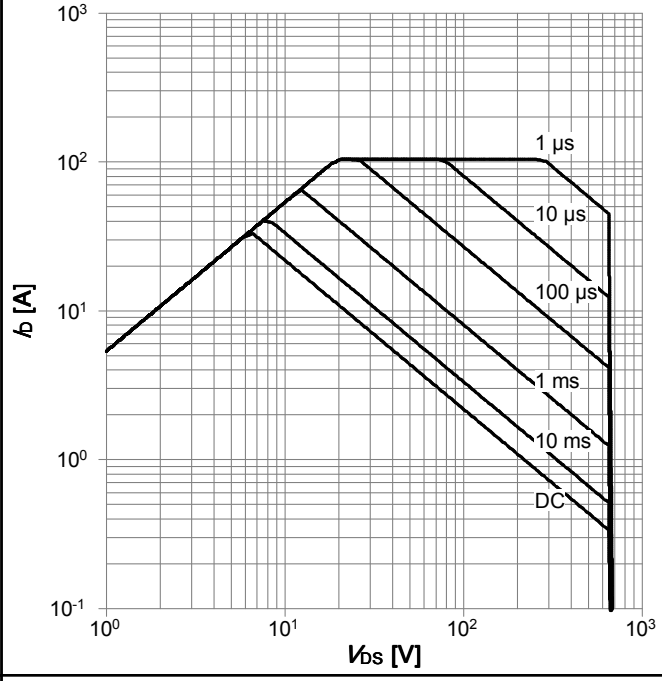
| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Diode forward voltage | $V_{SD}$ | | 0.9 | | V | $V_{GS}$ = 0V, $I_F$ = 26.3A, $T_j$ = 25°C |
| Reverse recovery time | $t_{rr}$ | | 180 | | ns | $V_R$ = 400V, $I_F$ = 26.3A, $dI_F/dt$ = 100A/µs |
| Reverse recovery charge | $Q_{rr}$ | | 1 | | µC | |
| Peak reverse recovery current | $I_{rrm}$ | | 10 | | A | |

# 5 Electrical characteristics diagrams

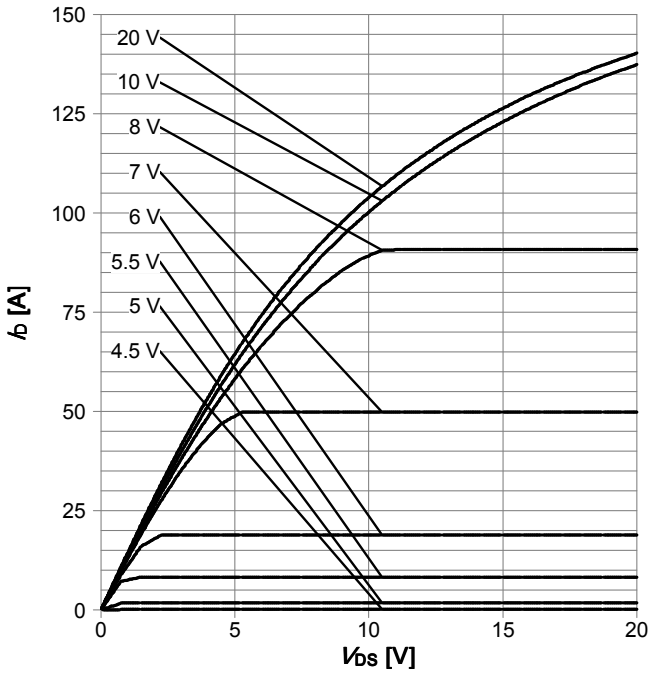
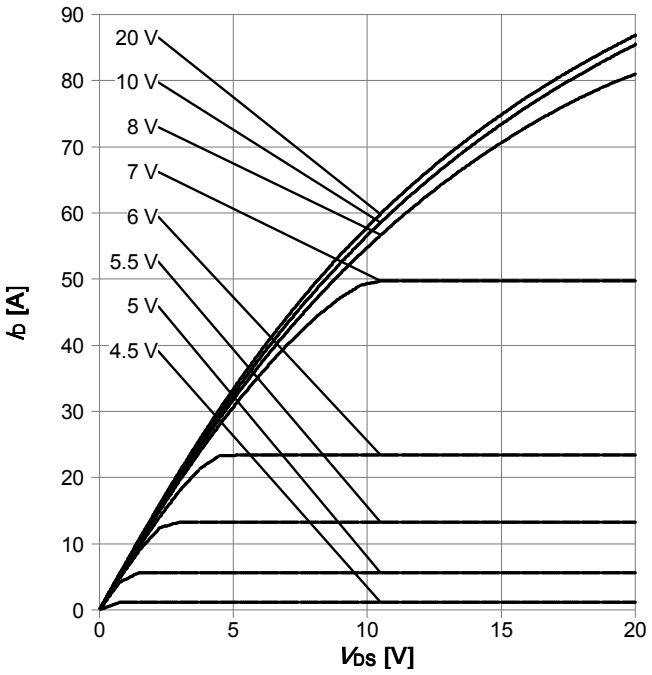
## Table 8

| Power dissipation (Non FullPAK) | Max. transient thermal impedance (Non FullPAK) |
|---|---|
|  |  |
| $P_{tot}=f(T_C)$ | $Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$ |

## Table 9

| Safe operating area $T_C$=25°C (Non FullPAK) | Safe operating area $T_C$=80°C (Non FullPAK) |
|---|---|
|  |  |
| $I_D=f(V_{DS})$; $T_C$=25 °C; Vgs>7,5V; $D$=0; parameter: $t_p$ | $I_D=f(V_{DS})$; Vgs>7,5V; $T_C$=80 °C; $D$=0; parameter: $t_p$ |

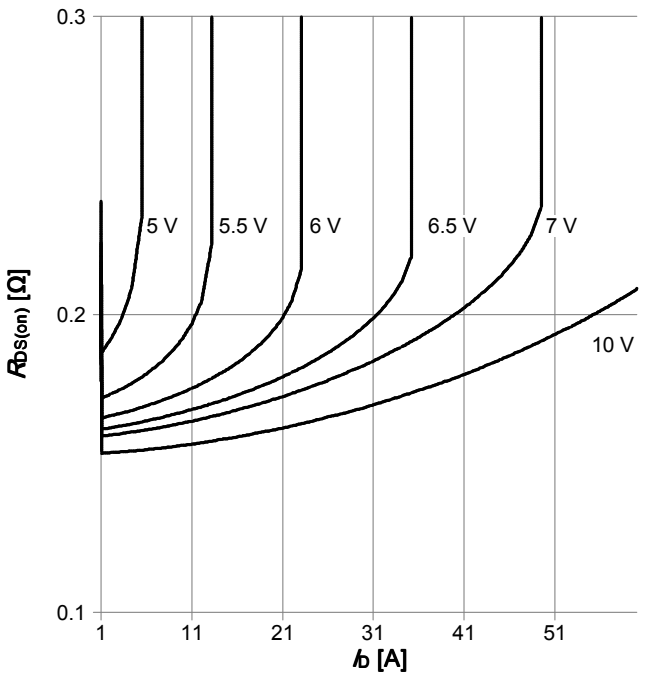
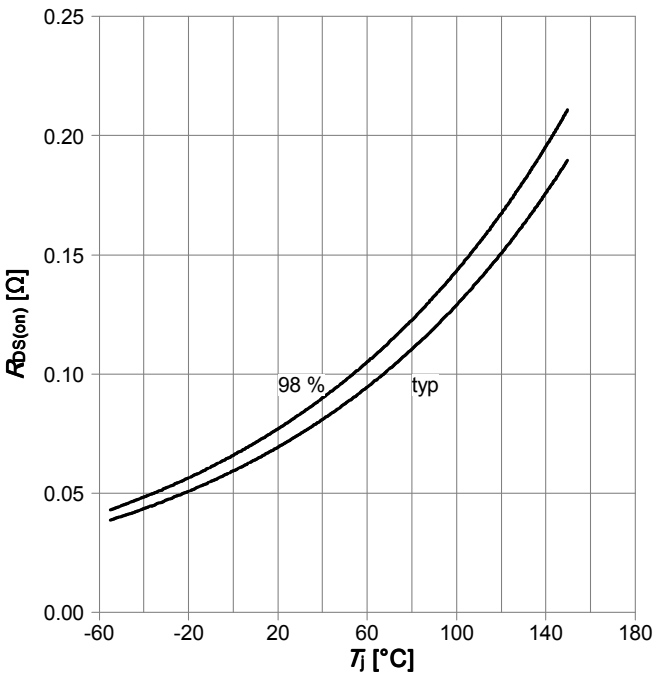
## Table 10

| Typ. output characteristics $T_C$=25°C | Typ. output characteristics $T_C$=125°C |
|---|---|
|  |  |
| $I_D$=f($V_{DS}$); $T_j$=25 °C; parameter: $V_{GS}$ | $I_D$=f($V_{DS}$); $T_j$=125 °C; parameter: $V_{GS}$ |

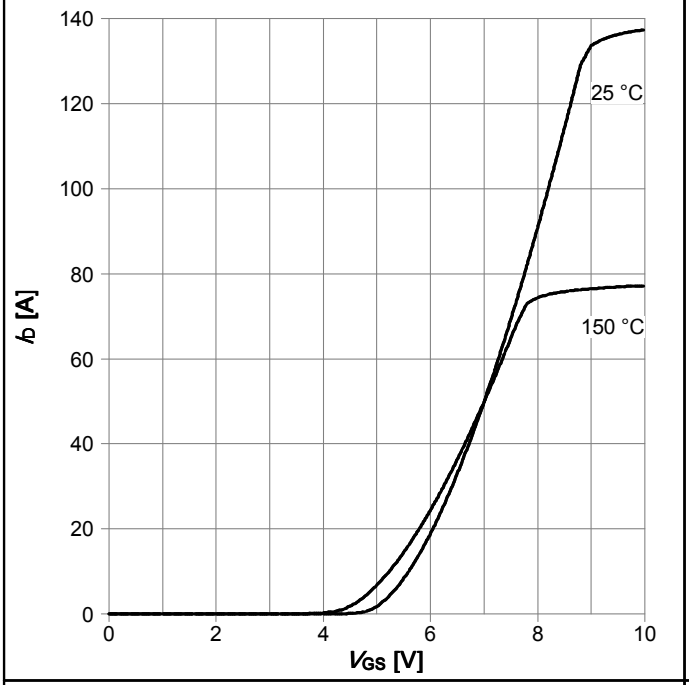
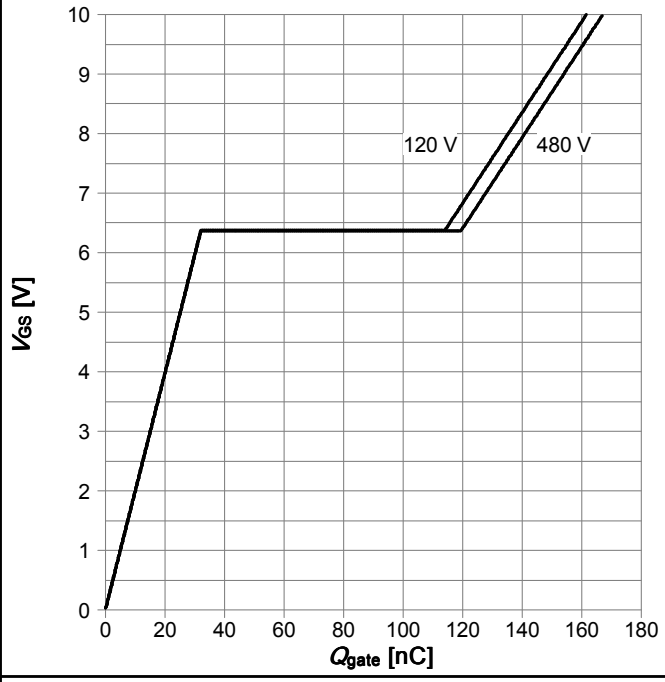




## Table 11

| Typ. drain-source on-state resistance | Drain-source on-state resistance |
|---|---|
|  |  |
| $R_{DS(on)}$=f($I_D$); $T_j$=125 °C; parameter: $V_{GS}$ | $R_{DS(on)}$=f($T_j$); $I_D$=17.6A; $V_{GS}$=10 V |

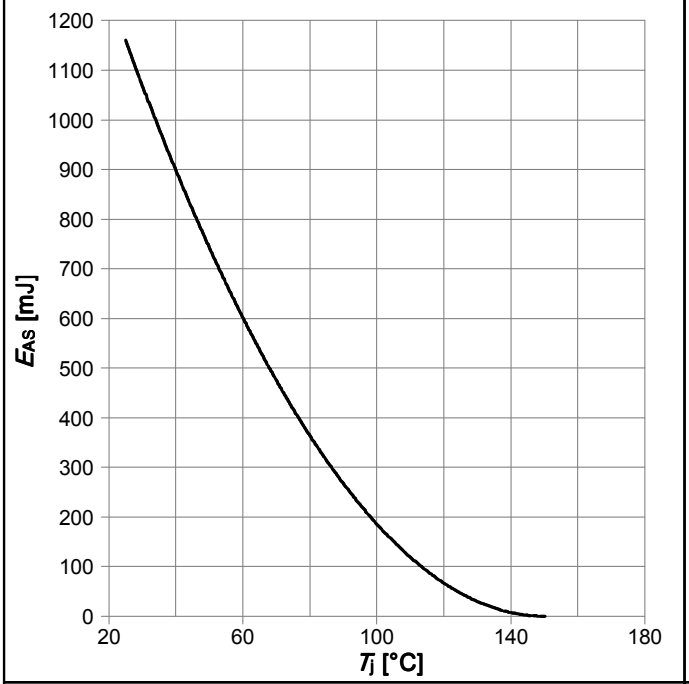
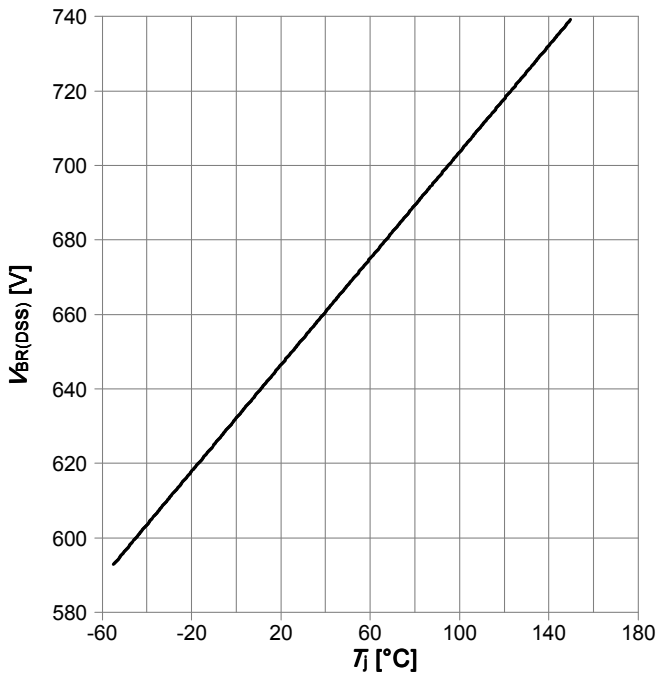
## Table 12

| Typ. transfer characteristics | Typ. gate charge |
|---|---|
|  |  |
| $I_D$=f($V_{GS}$); \|$V_{DS}$\|=20V; | $V_{GS}$=f($Q_{gate}$); $I_D$=26.3 A pulsed; parameter: $V_{DD}$ |

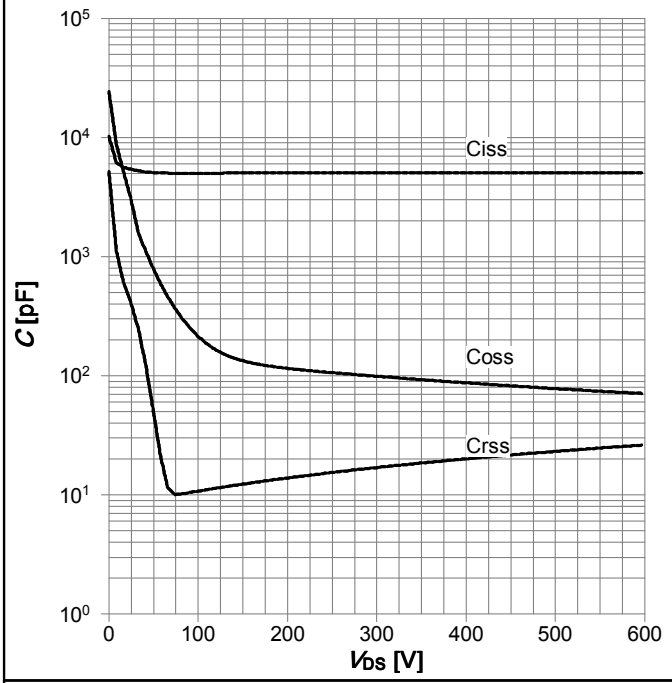
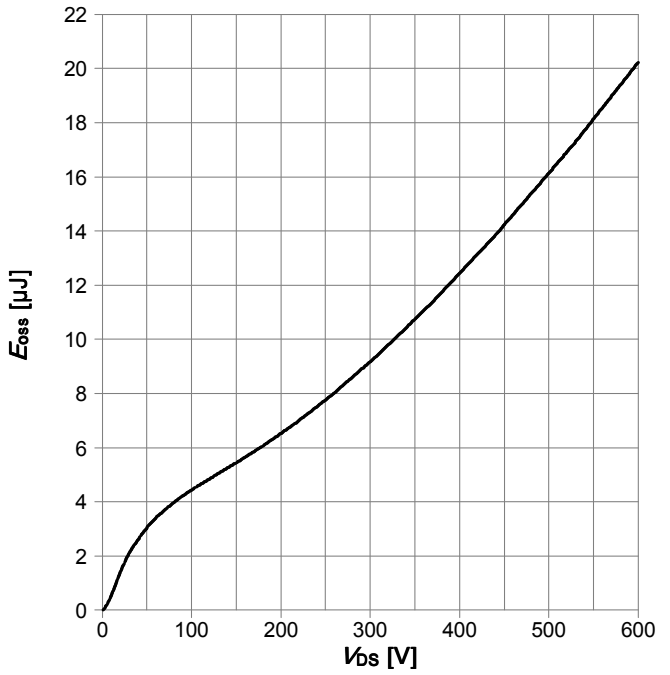




## Table 13

| Avalanche energy | Drain-source breakdown voltage |
|---|---|
|  |  |
| $E_{AS}$=f($T_j$); $I_D$=8.7 A; $V_{DD}$=50 V | $V_{BR(DSS)}$=f($T_j$); $I_D$=10 mA |

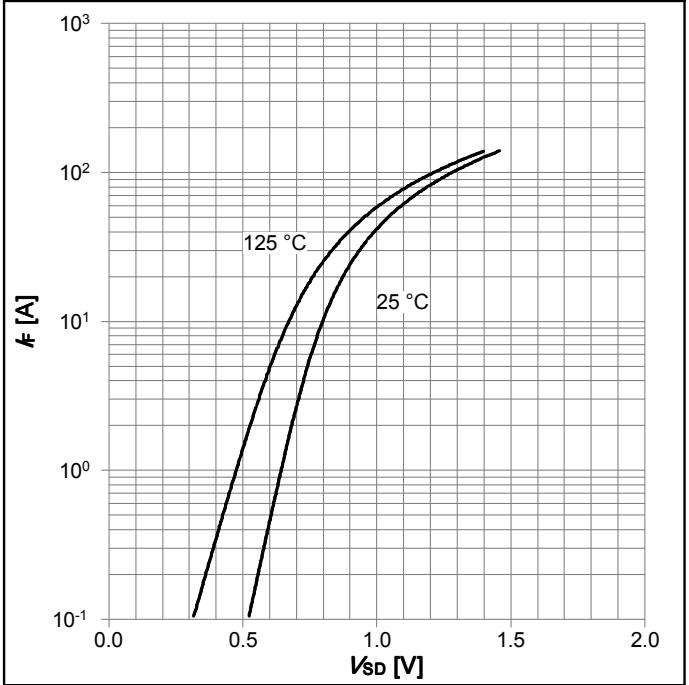
## Table 14

| Typ. capacitances | Typ. $C_{oss}$ stored energy |
|---|---|
|  |  |
| $C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz | $E_{oss}$=f($V_{DS}$) |





## Table 15

| Forward characteristics of reverse diode |
|---|
|  |
| $I_F$=f($V_{SD}$); parameter: $T_j$ |

# 6 Test Circuits

**Table 16 Diode_characteristics**

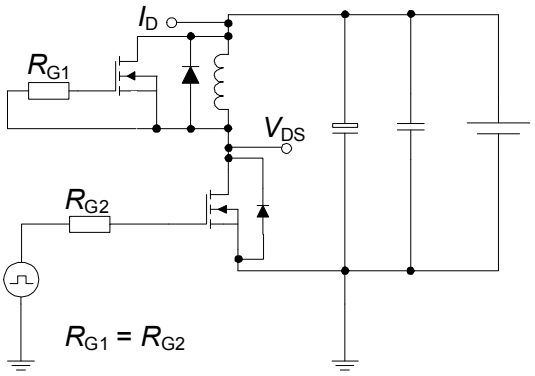
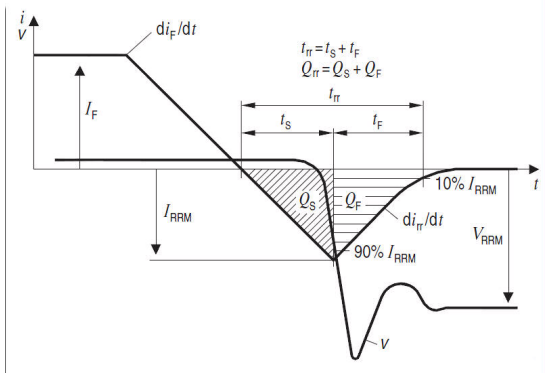
| Test circuit for diode characteristics | Diode recovery waveform |
|---|---|
|  |  |



**Table 17 Switching_times**

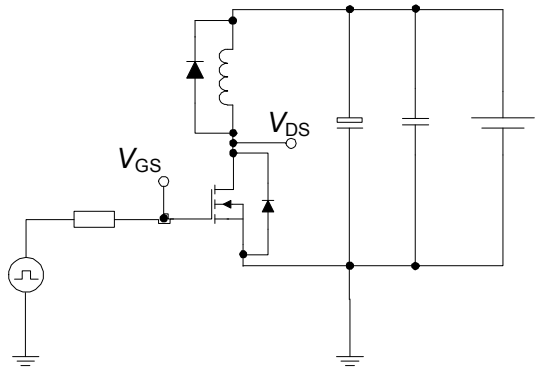
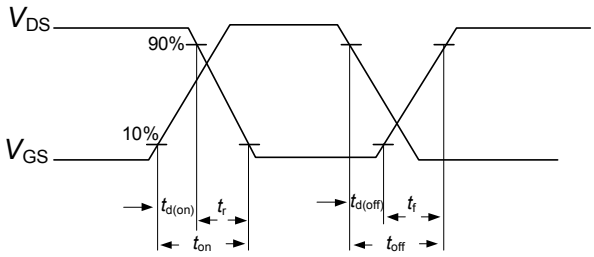
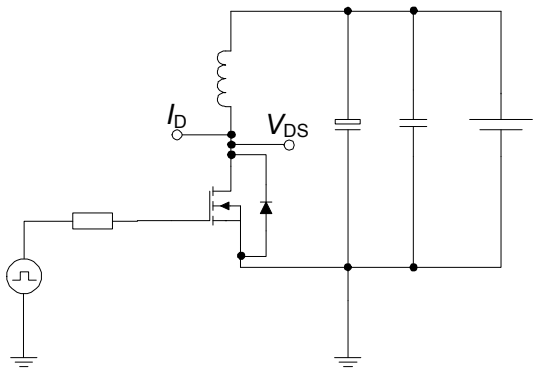
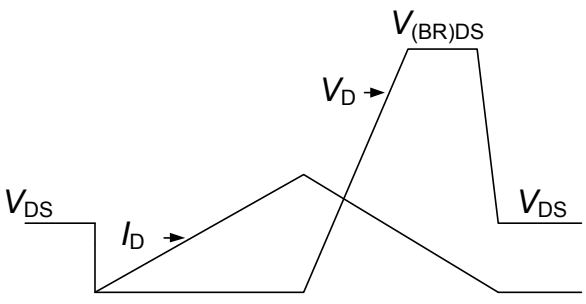
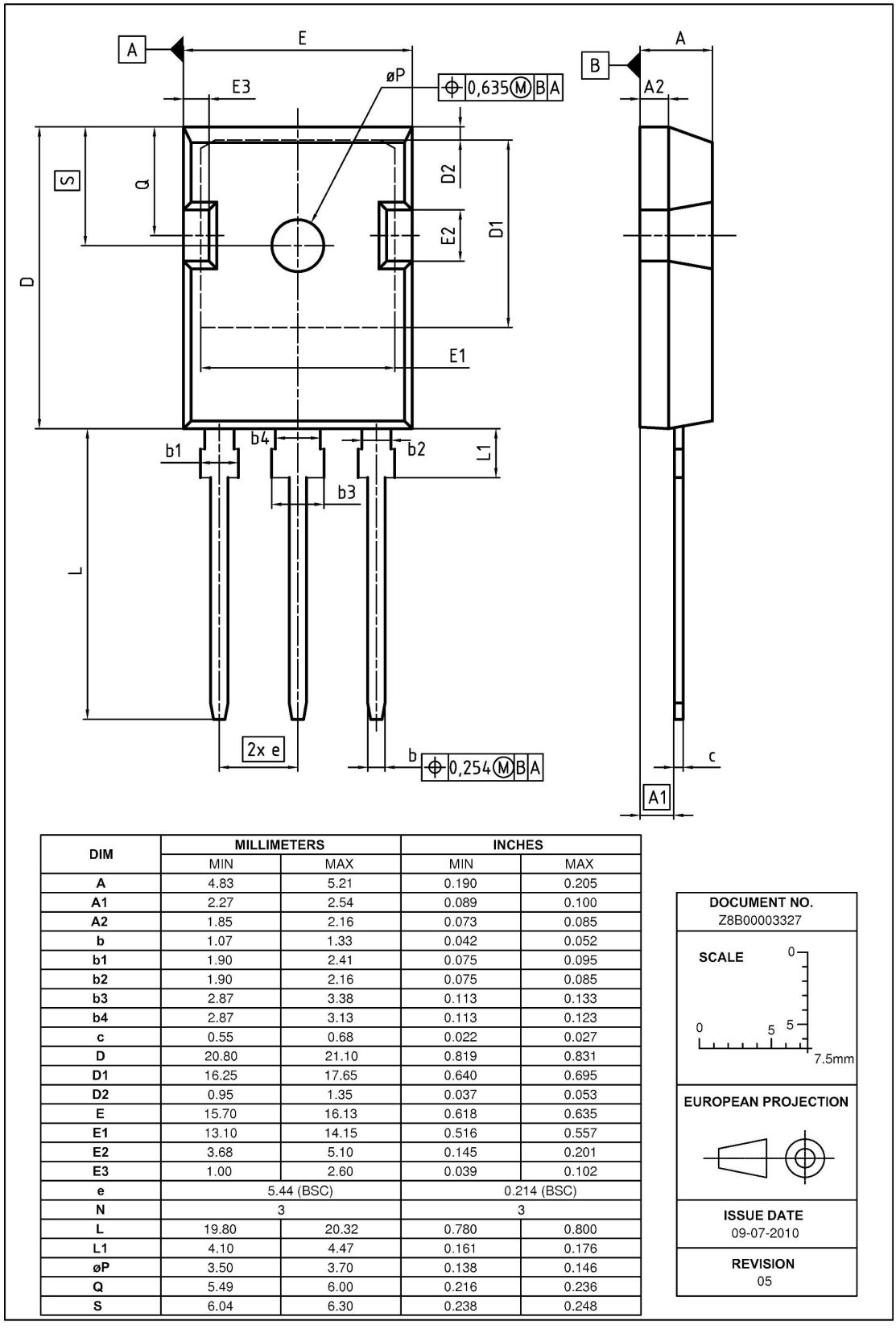
| Switching times test circuit for inductive load | Switching times waveform |
|---|---|
|  |  |



**Table 18 Unclamped_inductive**

| Unclamped inductive load test circuit | Unclamped inductive waveform |
|---|---|
|  |  |

## 7 Package Outlines




| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.83 | 5.21 | 0.190 | 0.205 |
| A1 | 2.27 | 2.54 | 0.089 | 0.100 |
| A2 | 1.85 | 2.16 | 0.073 | 0.085 |
| b | 1.07 | 1.33 | 0.042 | 0.052 |
| b1 | 1.90 | 2.41 | 0.075 | 0.095 |
| b2 | 1.90 | 2.16 | 0.075 | 0.085 |
| b3 | 2.87 | 3.38 | 0.113 | 0.133 |
| b4 | 2.87 | 3.13 | 0.113 | 0.123 |
| c | 0.55 | 0.68 | 0.022 | 0.027 |
| D | 20.80 | 21.10 | 0.819 | 0.831 |
| D1 | 16.25 | 17.65 | 0.640 | 0.695 |
| D2 | 0.95 | 1.35 | 0.037 | 0.053 |
| E | 15.70 | 16.13 | 0.618 | 0.635 |
| E1 | 13.10 | 14.15 | 0.516 | 0.557 |
| E2 | 3.68 | 5.10 | 0.145 | 0.201 |
| E3 | 1.00 | 2.60 | 0.039 | 0.102 |
| e | 5.44 (BSC) | | 0.214 (BSC) | |
| N | 3 | | 3 | |
| L | 19.80 | 20.32 | 0.780 | 0.800 |
| L1 | 4.10 | 4.47 | 0.161 | 0.176 |
| øP | 3.50 | 3.70 | 0.138 | 0.146 |
| Q | 5.49 | 6.00 | 0.216 | 0.236 |
| S | 6.04 | 6.30 | 0.238 | 0.248 |

DOCUMENT NO.
Z8B00003327

SCALE
0 5 5 7.5mm

EUROPEAN PROJECTION

ISSUE DATE
09-07-2010

REVISION
05

**Figure 1 Outline PG-TO 247, dimensions in mm/inches**

# 8 Appendix A

## Table 19 Related Links

- **IFX Design Tools:**
  http://www.infineon.com/cms/en/product/promopages/designtools/index.html
- **IFX CoolMOS Webpage:**
  http://www.infineon.com/cms/en/product/channel.html?channel=ff80808112ab681d0112ab6a628704d8

## Revision History

IPW65R080CFD

**Revision: 2011-09-27, Rev. 2.4**

| Previous Revision | | |
|---|---|---|
| Revision | Date | Subjects (major changes since last revision) |
| 2.1 | 2011-08-29 | update to CFD2 standard |
| 2.2 | 2011-09-15 | update pin naming |
| 2.3 | 2011-09-16 | release of new pin naming |
| 2.4 | 2011-09-27 | update the Igss test condition |

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